Specification Amendments

Amend the Abstract as follows:

In one embodiment of the invention, a phase selection unit for generating a recovered clock signal (SCLK), a phase select signal generator generates a ~~plurality of~~ phase select signals in response to a FWD signal and a BWD signal from a digital filter. The digital filter asserts the FWD signal if the phase of a SDIN (serial digital input) signal leads the phase of the recovered clock signal, and asserts the BWD signal if the phase of the SDIN (serial digital input) signal lags the phase of the recovered clock signal. A multiplexer ~~inputs~~ receives a ~~predetermined~~ number of given clock signals arranged in a predetermined phase order and outputs ~~a first output clock signal and a second output clock signal with the~~ selected first and second output clock signals, each being one of the given clock signals. A phase interpolator receives the selected first and second output clock signals from the multiplexer to generate the recovered clock signal having a phase that is phase interpolated between the phases of the first and second output clock signals~~. A multiplexer control circuit controls the multiplexer to select one of the given clock signals for each of the first and second output clock signals, depending on whether the phase select signals indicates that the FWD signal is asserted or that the BWD signal is asserted to properly adjust the phase of the recovered clock signal. With use of only one phase interpolator to generate the recovered clock signal (SCLK), consumption of power and chip space is minimized with the phase selection unit of the present invention.~~